PATENT ABSTRACTS OF JAPAN

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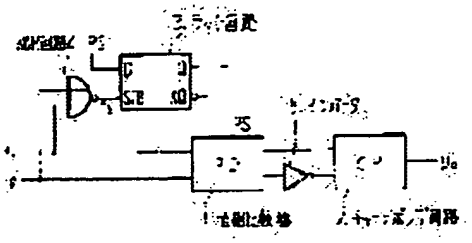
(71)Applicant : FUJITSU LTD
(72)Inventor : NAKAMICHI HIROTO
YAMAZAKI KOBO

(54) PLL FREQUENCY SYNTHESIZER

(57)Abstract:
PROBLEM TO BE SOLVED: To suppress delays in lock-up time by preventing frequency fluctuation at the time of turning into a power-save state.
SOLUTION: A reference signal fr and a comparison signal fp are inputted to a NOR circuit 4, and its output signal fs and a power save signal PS are inputted to a latch circuit 3. Since the latch circuit 3 is holding a previous 'H' level, even when the power save signal PS is at 'L' level, the power save signal PS controlling a charge pump circuit 2 to be inputted to a phase comparator 1 becomes 'H' level. Afterwards, at a time when both the reference signal fr and the comparison signal fp become the 'L' level, the output signal fs of the NOR circuit 4 is turned to the 'H' level and inputted to the latch circuit 3 as a strobe signal. Thus, a holding state is canceled, the power save signal PS inputted at present is outputted as it is, the charge pump circuit 2 is turned to the power-save state, and the lock-up time can be shortened.



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